Chenhe Yuan

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Education

University College London Sept 2022 - Jun 2026
MEng** (Integrated Master's) **in Electrical and Electronic Engineering

- GPA: **3.79**/4.0, *4-year combined Bachelor's and Master's degree program*
- **Relevant Courses**: Digital Electronics, Electromagnetic Theory and Semiconductor Devices, Photonics and Communication Systems, Analog and Power Electronics.

The University of Texas at Austin Aug 2024 - May 2025
Undergraduate Exchange, Electrical and Computer Engineering

- Spring Semester GPA: 3.5/4.0
- **Courses**: Computer Architecture, Algorithms, Compilers, Digital Electronics, Data Science Lab.

Research Experiences

Streaming Architecture Sparse 3D CNN Accelerator
Advisor: Prof. Lizy K. John, The University of Texas at Austin May 2025 – Dec 2025

- Implemented FPGA module in Vitis HLS, achieving 450 MHz synthesis frequency and validating pipeline timing.
- Developed streaming hierarchical bitmap construction mechanism to enable efficient sparse voxel filtering in 3D CNN workloads and reduce sparsity exploration overhead.
- Built a streaming pipeline with efficient on-chip buffer to support fast feature fetching.

Compute-in-Memory Architecture for In-Sensor CNN Evaluation
Advisor: Prof. Chao Li, Shanghai Jiao Tong University May 2024 – Oct 2024

- Designed a digital mimicry circuit emulating an analog-domain crossbar memristor array.
- Implemented the design targeting the Xilinx Zynq-7000 FPGA development board.
- Simulated and evaluated its performance across multiple configurations and representative workloads.

Embedded Acceleration Module for CNN Convolution
Advisor: Prof. Tinghuan Chen, The Chinese University of Hong Kong (Shenzhen) Jun 2023 – Oct 2023

- Contributed to FPGA IP design using the Winograd algorithm, focusing on reducing multiplications in convolution operations.
- Implemented element-wise real-time multiplication in Chisel HDL and SystemVerilog.
- Proposed synchronization and pipelining scheme for global control signals.

Project Experiences

Simulators for LC-3B Instruction Set Architecture (in C) Sep 2024 –Dec 2024
Advisor: Prof. Yale N. Patt, The University of Texas at Austin

- Built multiple LC-3B simulators at different abstraction levels (instruction-level, microarchitecture-level, virtual-memory, cycle-accurate) to validate functionality.
- Augmented the LC-3B microarchitecture to support virtual memory with user/system space separation.
- Implemented an assembler that translates LC-3B assembly programs into binary with starting addresses.

Publications

Enhancing the Efficiency of Embodied AI System with Squeezed Analog Perception Under Review
Submitted to *ISCA 26* (under review)

Cheng Xu, Prof. Chao Li, Prof. Xiaofeng Hou, ***Chenhe Yuan***, et al.

Working Paper on FPGA Accelerator In Preparation
Intended submission to *FCCM 26*

Chenhe Yuan, Ruihao Li, Prof. Lizy K. John, et al.

Skills

Programming & HDL: Vitis HLS, Chisel HDL, SystemVerilog, C/C++, Python, Java
Tools & Simulators: Timeloop/Accelergy, gem5, ChampSim, Accel-Sim, Vivado, Quartus, MATLAB